AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings include a complete set of formal drawings.

Attachment: Replacement sheets

REMARKS

Claims 2-41 are present in this application. Claim 1 has been canceled, and claim 8 has been rewritten into independent form. Claims 2-7 and 9-32 were withdrawn as a result of a restriction requirement. Subsequently, only claim 8 is the subject of the Office Action.

Applicants reserve the right to incorporate subject matter of original claim 1 (now included in claim 8) into withdrawn claims, as necessary.

New claims 33-41 have been added as claims dependent on claim 8.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Drawings

The Office Action indicates that several of the drawings were provided as informal drawings. Applicants provide a complete set of formal drawings attached hereto. Applicants request that the formal drawings be entered and that the drawing objection be withdrawn.

Title

The Office Action indicates that the title is not descriptive. Applicants provide herewith a revised title that reflects the elected claimed invention. Applicants request that the new title be entered.

Claim Objection

Claim 1 has been objected to. Applicants have rewritten claim 8 into independent form including subject matter of claim 1. In rewriting claim 8, grammatical errors in original claim 1 have been corrected. Applicants request that the objection be reconsidered and withdrawn in view of the claim as amended.

§ 102(b) Rejection

Claims 1 and 8 have been rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,731,598 (Kado). Applicants respectfully traverse this rejection.

Embodiments of the present invention covered by claim 8 (e.g., Figs. 9 and 10; Specification at para. 0298 to 0305) are directed to a memory in which at least two memory cells (M1, M2, etc.) each including a resistance-changing function body (e.g. Fig. 1: 113; 904/905, 1004, 1014, 1024) and arranged in a direction parallel to a substrate (para. 0298; 900).

The resistance-changing function body of each of the memory cells (Figs. 1-5) includes, among other things, an object made of a first substance and interposed between a first electrode and a second electrode, and a plurality of particles made of a second substance. The first substance makes an electrical barrier against the second substance.

This claimed feature covers the aspect that, "the regions that perform the memory operation in the memory function body 904 are limited to regions 905 and 905 which are interposed between the bit contact 901 and the drain regions 903 and 903 and to which a voltage is applied as shown in Fig. 9B. The memory function body 904 is basically an insulator although it contains conductive particles. Therefore, the remaining region (corresponding to the portion located between the regions 905 and 905) to which no effective voltage is applied in the memory function body 904 performs no memory operation." (Specification at para. 0299).

Further, according to the present specification, "Drain regions 903 and 903 of the memory cells M2 and M3 are isolated apart in the transverse direction, and one memory function body 904 (same as the foregoing particle container 113) and one bit contact 901 are formed over those drain regions 903 and 903. That is, the memory function body 904 is formed integrally continuously in the transverse direction so as to be in contact with the two drain regions 903 and 903." (Specification at para. 0298).

This feature is covered by the claim as, objects made of the first substance of memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed.

Kado discloses an implementation of a single electron tunnel device that is a solution to a problem of tunnel leak current found to occur between a gate electrode and a semiconductor substrate. In particular, Kado discloses a single electron tunnel device in which,

"since metal or semiconductor particles are dispersed in the electrically insulating thin film with high density, electrons tunnel through the gaps between the metal or semiconductor particles when a voltage is applied between electrodes, allowing a so-called tunnel current to flow in the electrically insulating thin film. Accordingly, by forming electrodes in contact with the electrically insulating thin film with metal and semiconductor particles dispersed therein and applying a voltage between the electrodes, a multiple tunnel junction structure is formed where electrons flow between the electrodes through a number of tunnel junctions connected in series, and thus a single electron tunnel device using the Coulomb blockage effect is realized. Since the metal or semiconductor particles can be dispersed in the electrically insulating thin film comparatively uniformly, a multiple tunnel junction structure with a controlled configuration can be easily obtained." (col. 3, ls. 44-61).

Kado discloses the single electron tunnel device can be configured as a transistor or a memory depending on the configuration of the electrodes (col. 12, ln.67 to col. 13, ln. 2; col. 13, ls. 19-21). Kado discloses examples of the single electron device showing the associated source electrode and drain electrode.

The Office Action alleges that Kado "discloses the patterning of multiple devices during one sputtering process" (citing col. 6, lns. 27-36). The Office Action alleges that a section at col. 6, lines 19-25, teaches fabrication of "at least two memory resistance-changing function bodies" where the objects made of the first substance of memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed."

Applicants submit that Kado discloses examples of one memory cell (having an associated source electrode and an associated drain electrode), but does not disclose a device having "at least two memory cells." Consequently, Kado does not disclose the claimed feature of

"objects made of the first substance of memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed."

Claim 8 requires at least two memory cells including a resistance-changing function body are arranged in a direction parallel to a substrate (see, for example, Fig. 9A); and the objects made of the first substance of memory cells mutually adjacent in the direction parallel to the substrate are integrally continuously formed. With this arrangement, the process of separating the resistance-changing function body every cell can be eliminated, and therefore, the productivity is improved. (Specification at para. 0037). In other words, the arrangement of the resistance-changing function body for adjacent memory cells is such that the resistance-changing function body does not have to be separated for every cell. Subsequently, the occupation area per cell is reduced, and the integration density is improved (Specification at paras. 0300, 0305).

Kado discloses only a total of two, or three, electrodes formed for each multiple tunnel junction layer 6, constituting a single memory device. In particular, Kado does not disclose, for example, a memory in which the electrical insulating layer is integrally continuously formed over a pair of electrodes between mutually adjacent memory cells.

For at least these reasons, Applicants submit that Kado fails to teach each and every claimed element. Accordingly, Applicants request that the rejection be reconsidered and withdrawn.

New Claims

Claims 33 to 41 have been added. New claims 33-41 cover further features of the memory of claim 8. Applicants submit that at least for the reasons above for claim 8, new claims 33 to 41 are patentable as well.

Conclusion

In view of the above remarks, it is believed that claims are allowable.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact **Robert Downs** Reg. No. 48,222 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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Attachments

REPLACEMENT SHEET